Current Mode PWM Controller

FEATURES

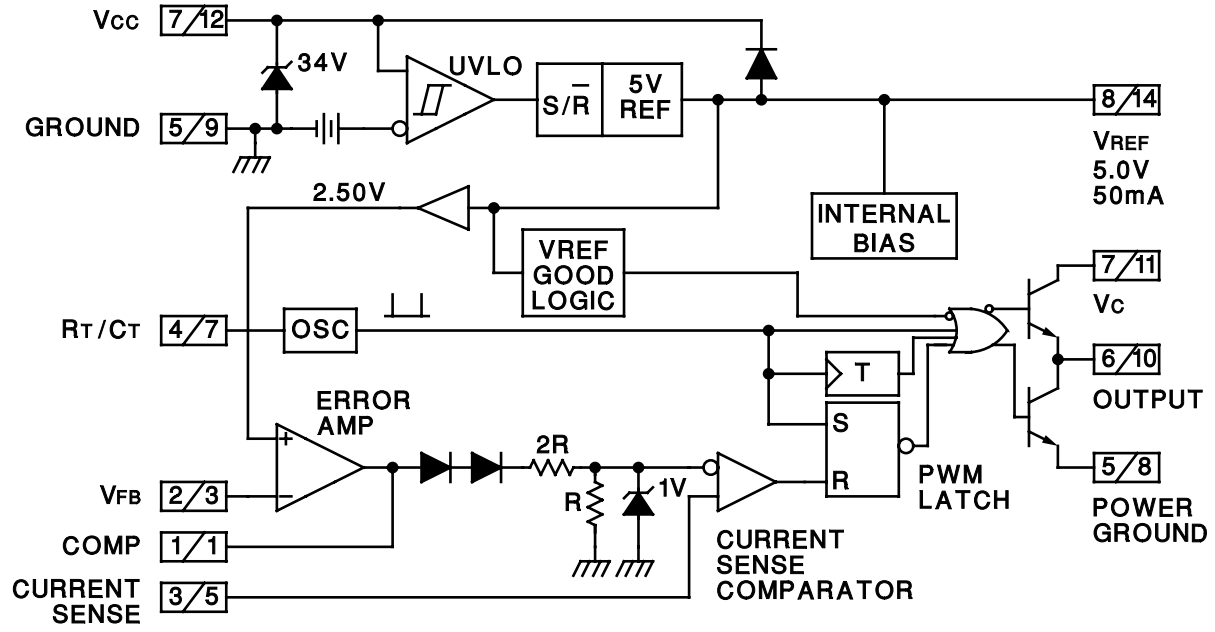
- Optimized For Off-line And DC To DC Converters
- Low Start Up Current (<1mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500khz Operation
- Low RO Error Amp

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4V and 7.6V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 and CFP-14 Pin Number.
Note 2: Toggle flip flop used only in 1844 and 1845.

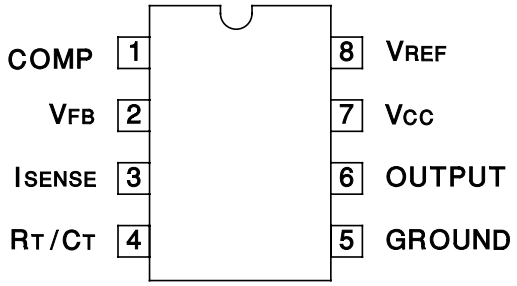
ABSOLUTE MAXIMUM RATINGS(Note 1)

Supply Voltage (Low Impedance Source) 30V
Supply Voltage (I_{CC} < 30mA) . . . . . Self Limiting
Output Current. . . . . ±1A
Output Energy (Capacitive Load) . . . . . 5 µJ
Analog Inputs (Pins 2, 3). . . . . -0.3V to +6.3V
Error Amp Output Sink Current . . . . . 10 mA
Power Dissipation at $T_A \leq 25°C$ (DIL–8) . . . . . 1 W
Power Dissipation at $T_A \leq 25°C$ (SOIC-14) . . . . . 725 mW
Storage Temperature Range. . . . . -65°C to +150°C
Junction Temperature Range . . . . . -55°C to +150°C
Lead Temperature (soldering, 10 seconds). . . . . 300°C

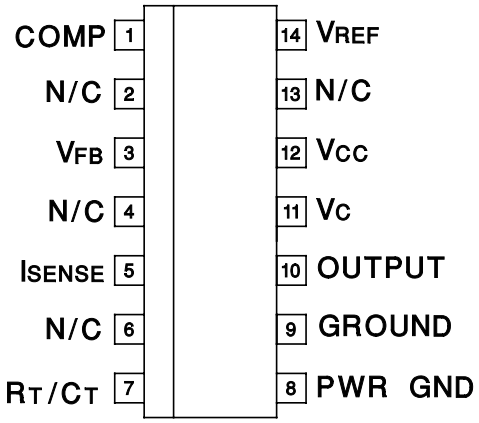
Note 1: All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

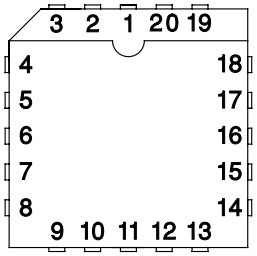
DIL-8, SOIC-8 (TOP VIEW)
N or J Package, D8 Package



SOIC-14, CFP-14. (TOP VIEW)
D or W Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
COMP	2
N/C	3
N/C	4
V_{FB}	5
N/C	6
I_{SENSE}	7
N/C	8
N/C	9
R_T/C_T	10
N/C	11
PWR GND	12
GROUND	13
N/C	14
OUTPUT	15
N/C	16
V_C	17
V_{CC}	18
N/C	19
V_{REF}	20

DISSIPATION RATING TABLE

Package	TA ≤ 25°C Power Rating	Derating Factor Above TA ≤ 25°C	TA ≤ 70°C Power Rating	TA ≤ 85°C Power Rating	TA ≤ 125°C Power Rating
W	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW